Amendments to the Claims:

1. (currently amended) A timing circuit comprising:

a clock generator;

a comparator for comparing an inputted control voltage and a reference voltage, wherein said comparator receives a first clock signal outputted from said clock generator and is operated only for a time corresponding to a short pulse width of said first clock signal;

a retaining circuit for retaining an output of said comparator; and

a circuit for producing timing pulses as an output thereof based on an output of said retaining circuit and clock signals outputted from said clock generator.

2. (canceled) A timing circuit according to claim 1, wherein said comparator receives a first clock signal outputted from said clock generator and is operated only for a time corresponding to a short pulse width of said first clock signal.

3. (original) A timing circuit according to claim 1, wherein said circuit for producing said timing pulses comprises:

a counter for receiving the output of said retaining circuit and a first clock signal outputted from said clock generator; and

a logic circuit for receiving an output of said counter and a second clock signal outputted from said clock generator.

4. (original) A timing circuit according to claim 3, further comprising a circuit for receiving the output of said retaining circuit and sending a reset signal to said counter.

5. (original) A timing circuit according to claim 1, wherein said comparator comprises:

a first comparator for receiving a first reference voltage and said control voltage; and

a second comparator for receiving a second reference voltage and said control voltage.

6. (original) A timing circuit according to claim 5, wherein said retaining circuit comprises:

a first latch circuit for receiving an output of said first comparator; and

a second latch circuit for receiving an output of said second comparator.

7. (original) A timing circuit according to claim 3, wherein said logic circuit comprises an AND circuit.

8. (original) A timing circuit for producing clocks variable depending on a temperature, said timing circuit comprising a detection circuit that can detect the temperature at a predetermined sampling period, wherein said detection circuit is operated only for a time corresponding to a short pulse width of a clock signal that changes its level at said sampling period, thereby to detect the temperature.

9. (original) A timing circuit for controlling a refresh period of a DRAM depending a temperature, said timing circuit comprising a detection circuit that can detect the temperature at a predetermined sampling period, wherein said detection circuit is operated only for a time corresponding to a short pulse width of a clock signal that changes its level at said sampling period, thereby to detect the temperature.

10. (original) A timing circuit according to claim 9, wherein said sampling period is a period determined by T x n where T represents a refresh period required at the maximum operating temperature of the DRAM and n represents an arbitrary natural number.

11. (currently amended) A method for changing a clock period, comprising:

(a) a step of preparing a reference clock signal;

(b) a step of detecting a temperature at a predetermined sampling period and only for a time corresponding to a short pulse width of a clock signal that changes its level at said sampling period; and

(c) a step of changing a period of said reference clock signal depending on said detected temperature.

12. (canceled) A method according to claim 11, wherein said step (b) comprises a step of detecting a temperature only for a time corresponding to a short pulse width of a clock signal that changes its level at said sampling period.

13. (original) A method according to claim 11, wherein said step (c) comprises a step of producing a clock signal having a longer period by increasing the number of pulses decimated from said reference clock signal depending on dropping of said detected temperature.

14. (original) A method according to claim 11, wherein said sampling period is a period determined by T x n where T represents the period of said reference clock signal and n represents an arbitrary natural number, and said natural number n is set to a large value when the changing speed of the temperature is slow, and to a small value when the changing speed of the temperature is fast.